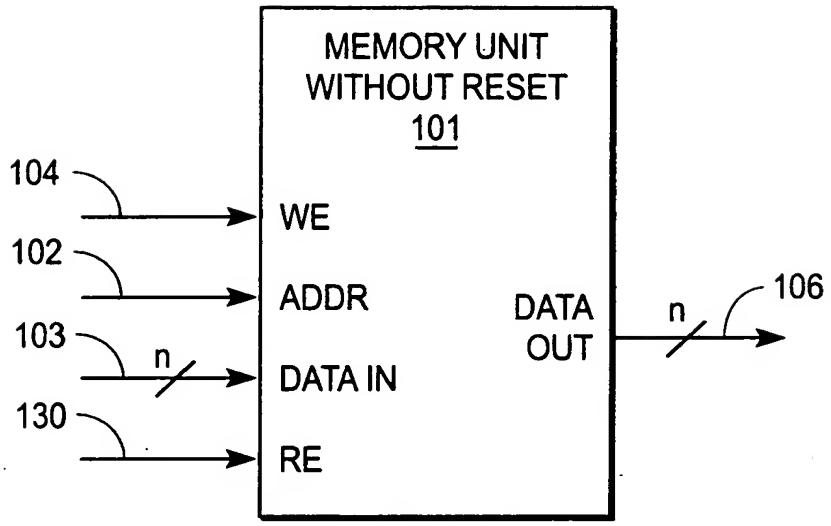

FIG. 1

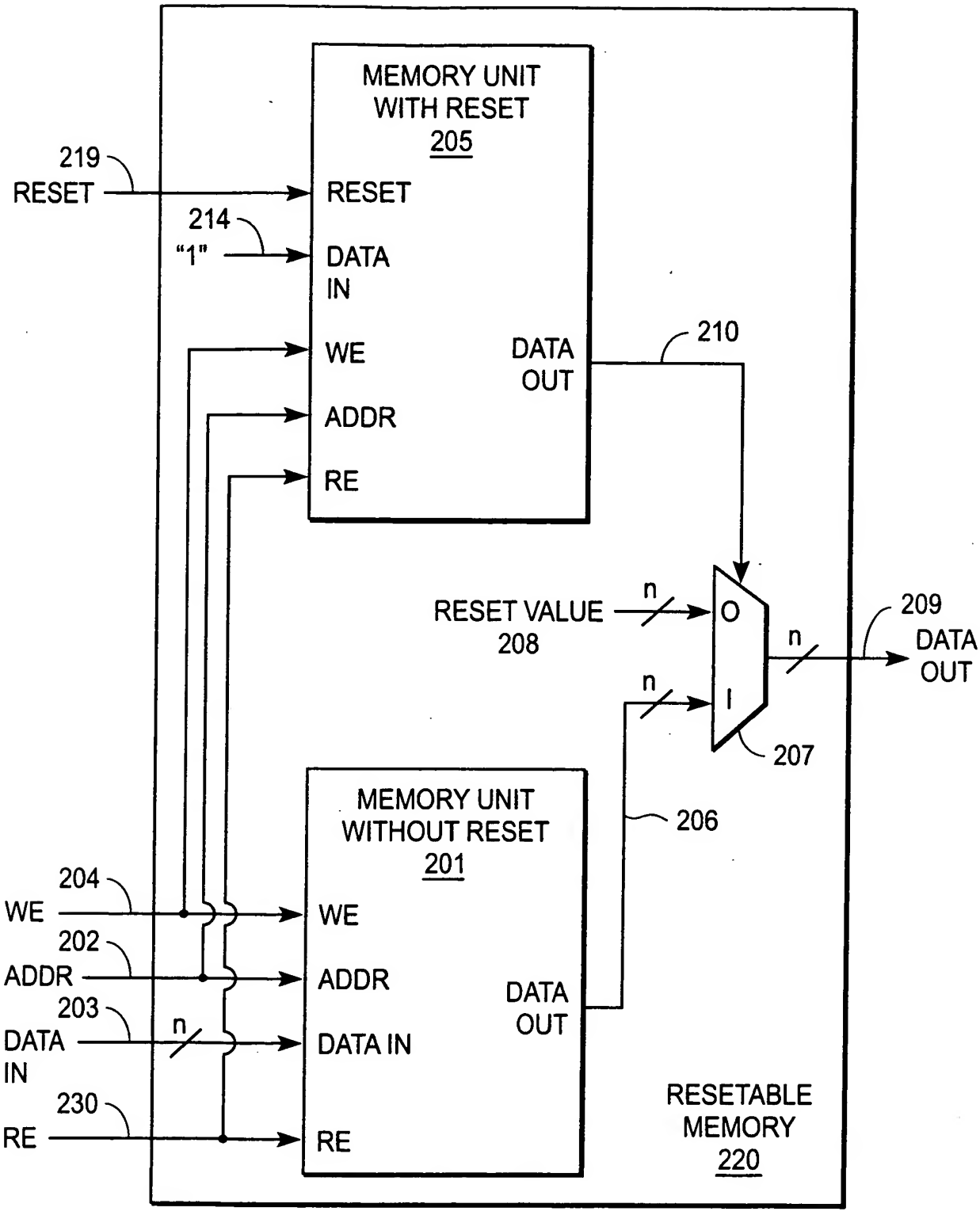
MEMORY UNIT
WITH RESET
205
219
RESET
RESET
214
"1"
DATA
IN
WE
ADDR
RE
DATA
OUT
210
RESET VALUE
208
n
O
I
n
n
209
DATA
OUT
207
MEMORY UNIT
WITHOUT RESET
201
206
204
WE
WE
202
ADDR
ADDR
203
DATA
IN
n
DATA IN
DATA
OUT
230
RE
RE
RESETABLE
MEMORY
220

FIG. 2A

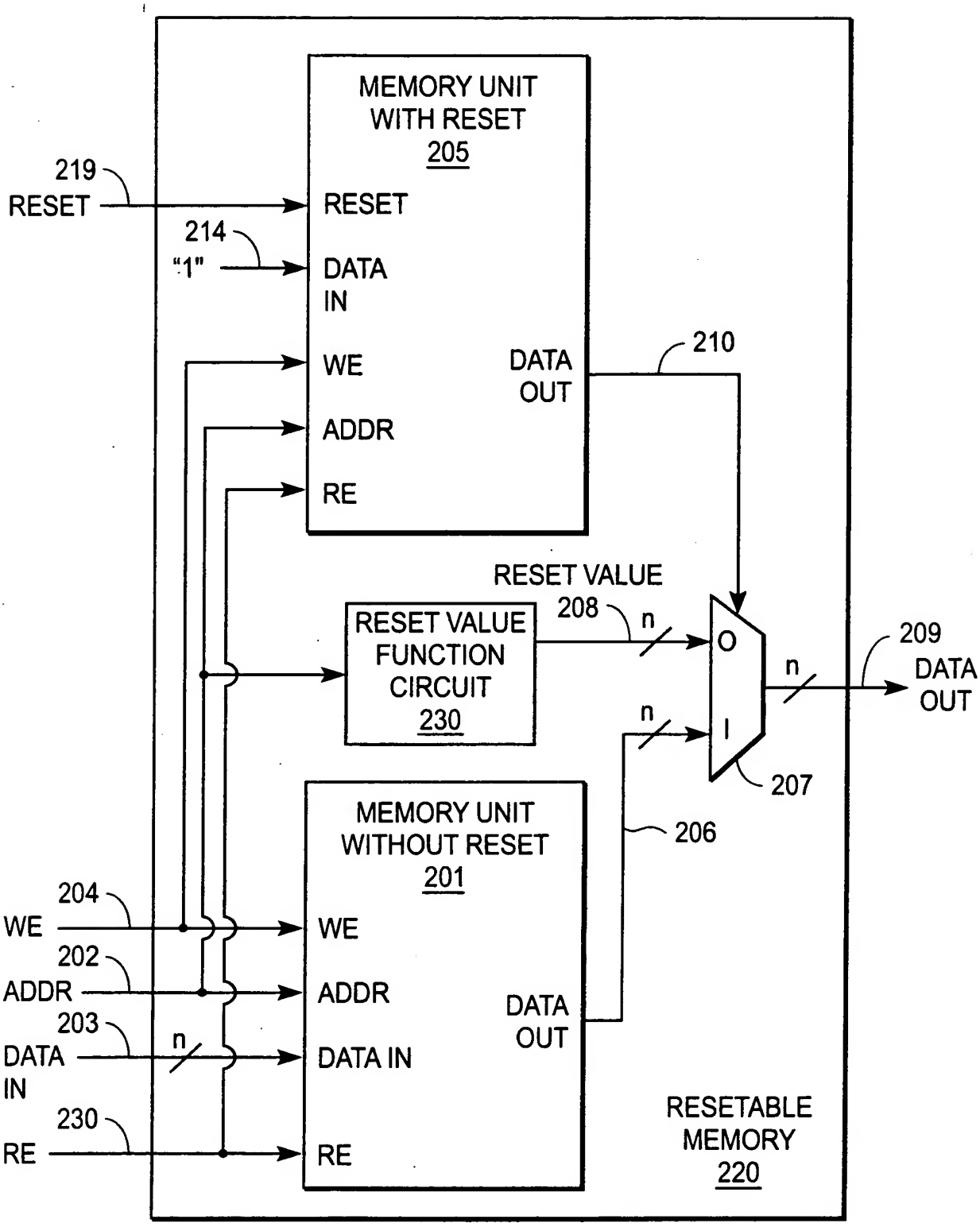
MEMORY UNIT
WITH RESET
205
219
RESET
RESET
214
"1"
DATA
IN
WE
ADDR
RE
DATA
OUT
210
RESET VALUE
208
n
RESET VALUE
FUNCTION
CIRCUIT
230
O
I
n
n
209
DATA
OUT
207
206
MEMORY UNIT
WITHOUT RESET
201
204
WE
WE
202
ADDR
ADDR
203
DATA
IN
n
DATA IN
DATA
OUT
230
RE
RE
RESETABLE
MEMORY
220

FIG. 2B

```
module synReset(data_in, addr, reset, we, clk, data_out);

parameter data_width = 1024;
parameter addr_width = 10;
parameter RAMsize = 8;
parameter reset_value = 8'D0;

input [data_width-1:0] data_in;
input [addr_width-1:0] addr;
input reset, we, clk;
output [data_width-1:0] data_out;

integer i;
reg [data_width-1:0] mem [RAMsize-1:0];
wire [data_width-1:0] data_out;
//synthesis loop_limit 2000
always @(posedge clk)
begin
        if(reset == 1'b1)
        begin
                for (i=0; i < RAMsize ; i=i+1)
                        begin
                                mem[i] = reset_value;
                        end
        end else if(we == 1'b1)
        begin
                        mem[addr] = data_in;
        end
end
assign data_out = mem[addr];
endmodule
```

FIG. 2C

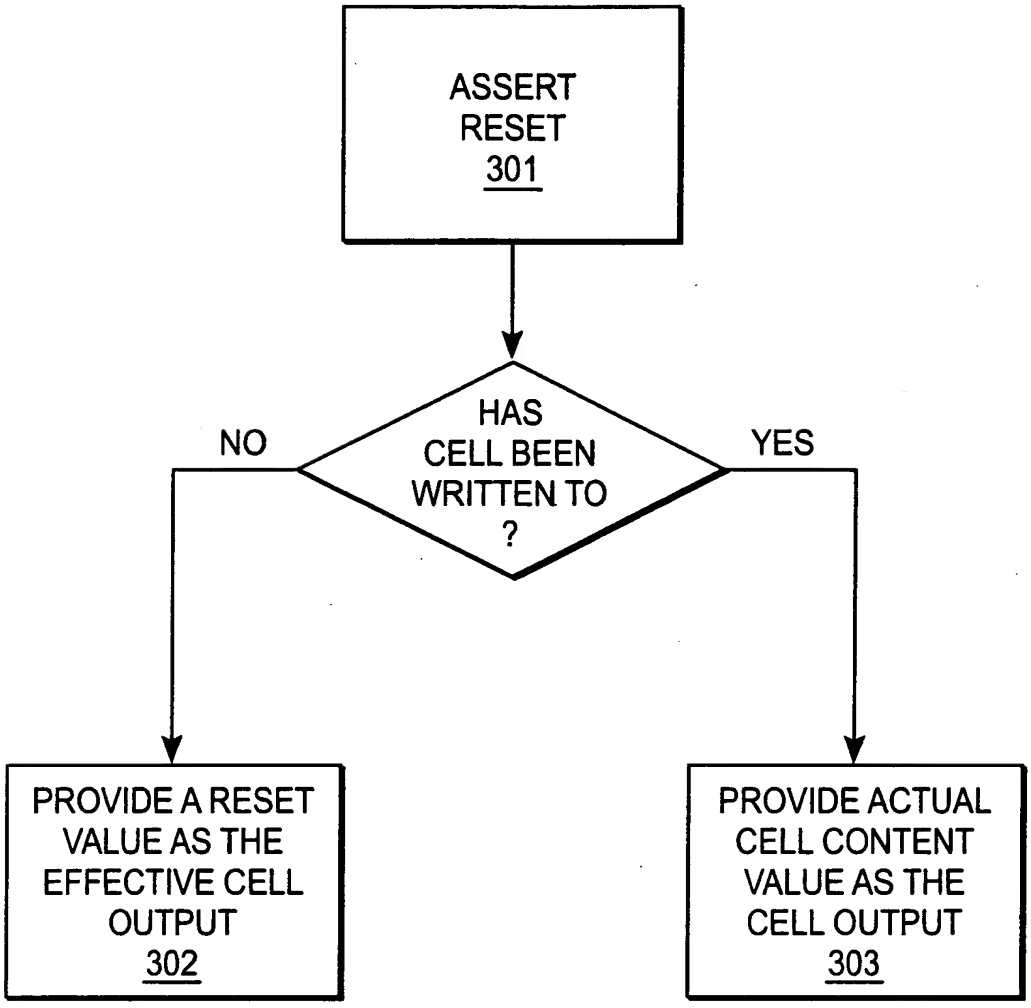
ASSERT
RESET
301
HAS
CELL BEEN
WRITTEN TO
?
NO
YES
PROVIDE A RESET
VALUE AS THE
EFFECTIVE CELL
OUTPUT
302
PROVIDE ACTUAL
CELL CONTENT
VALUE AS THE
CELL OUTPUT
303

FIG. 3

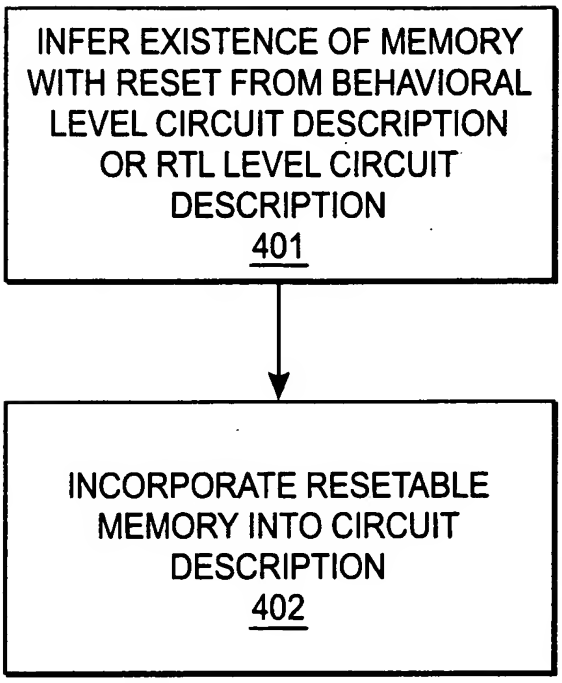
INFER EXISTENCE OF MEMORY WITH RESET FROM BEHAVIORAL LEVEL CIRCUIT DESCRIPTION OR RTL LEVEL CIRCUIT DESCRIPTION
401
INCORPORATE RESETABLE MEMORY INTO CIRCUIT DESCRIPTION
402

FIG. 4

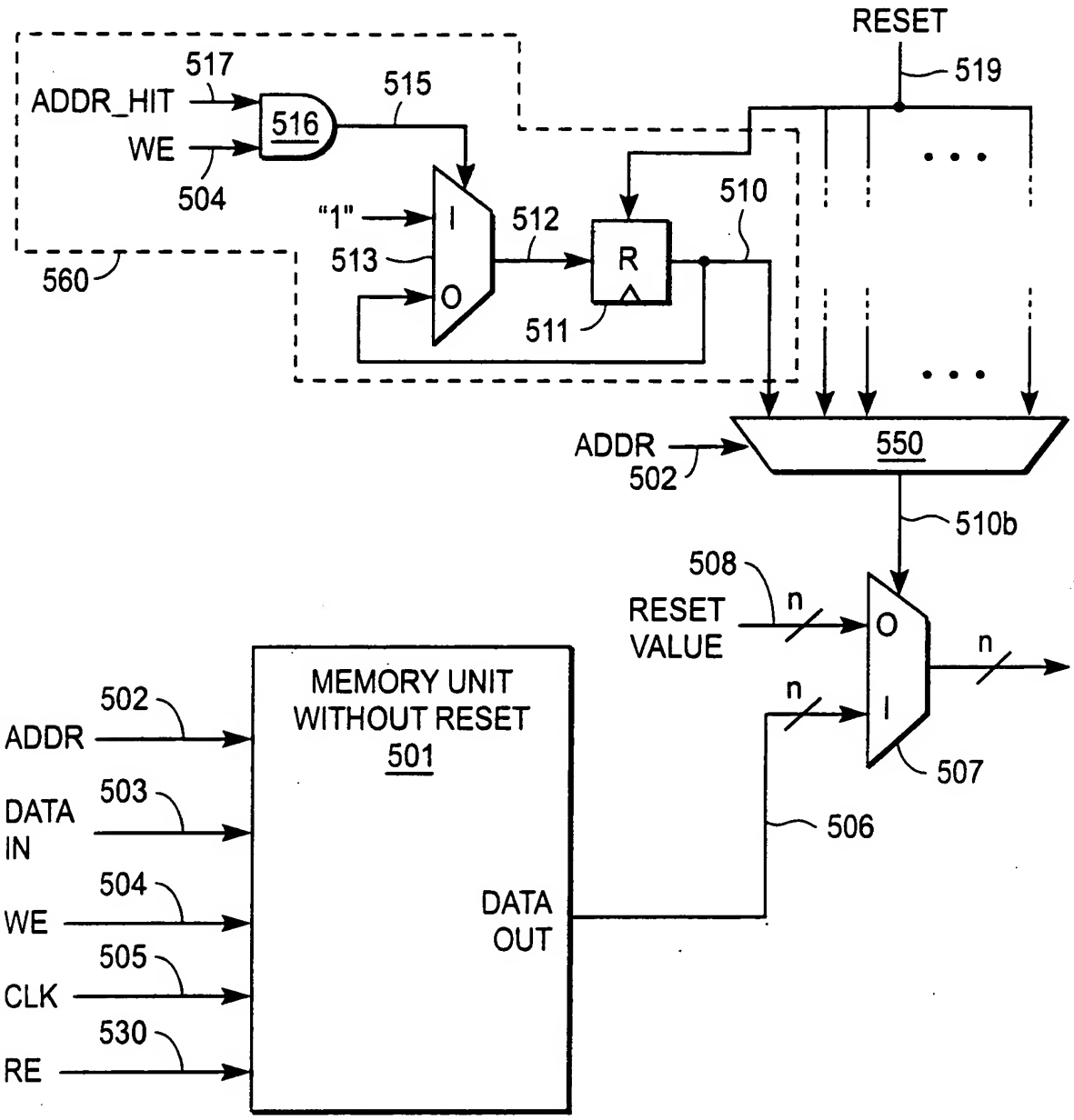
RESET
519
517
ADDR_HIT
515
516
WE
504
"1"
513
I
O
512
R
510
511
560
ADDR
502
550
510b
508
RESET
VALUE
n
O
I
n
n
507
506
MEMORY UNIT
WITHOUT RESET
501
502
ADDR
503
DATA
IN
504
WE
505
CLK
530
RE
DATA
OUT

FIG. 5

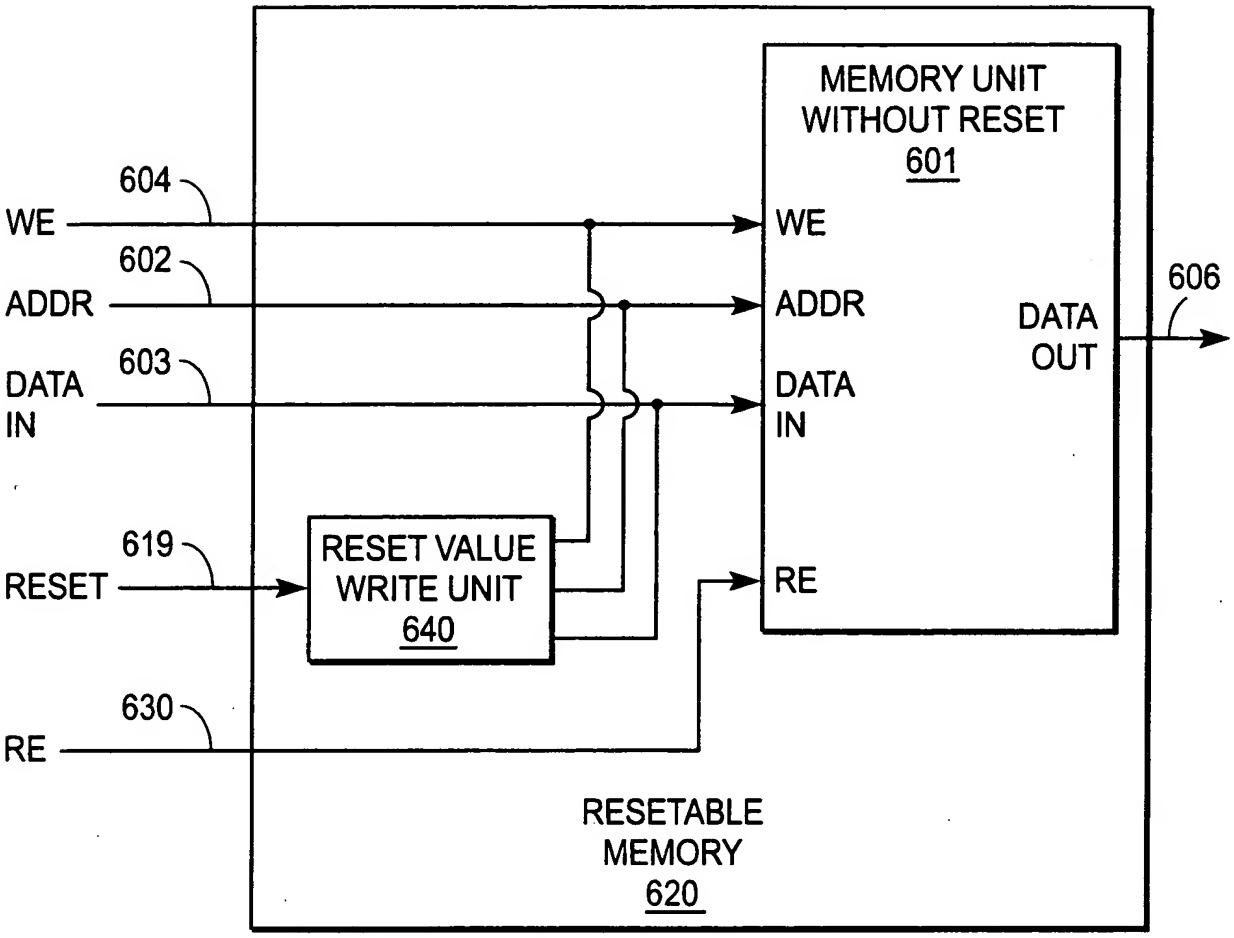
MEMORY UNIT
WITHOUT RESET
601
604
WE
602
ADDR
603
DATA
IN
619
RESET
630
RE
RESET VALUE
WRITE UNIT
640
WE
ADDR
DATA
IN
RE
606
DATA
OUT
RESETABLE
MEMORY
620

FIG. 6

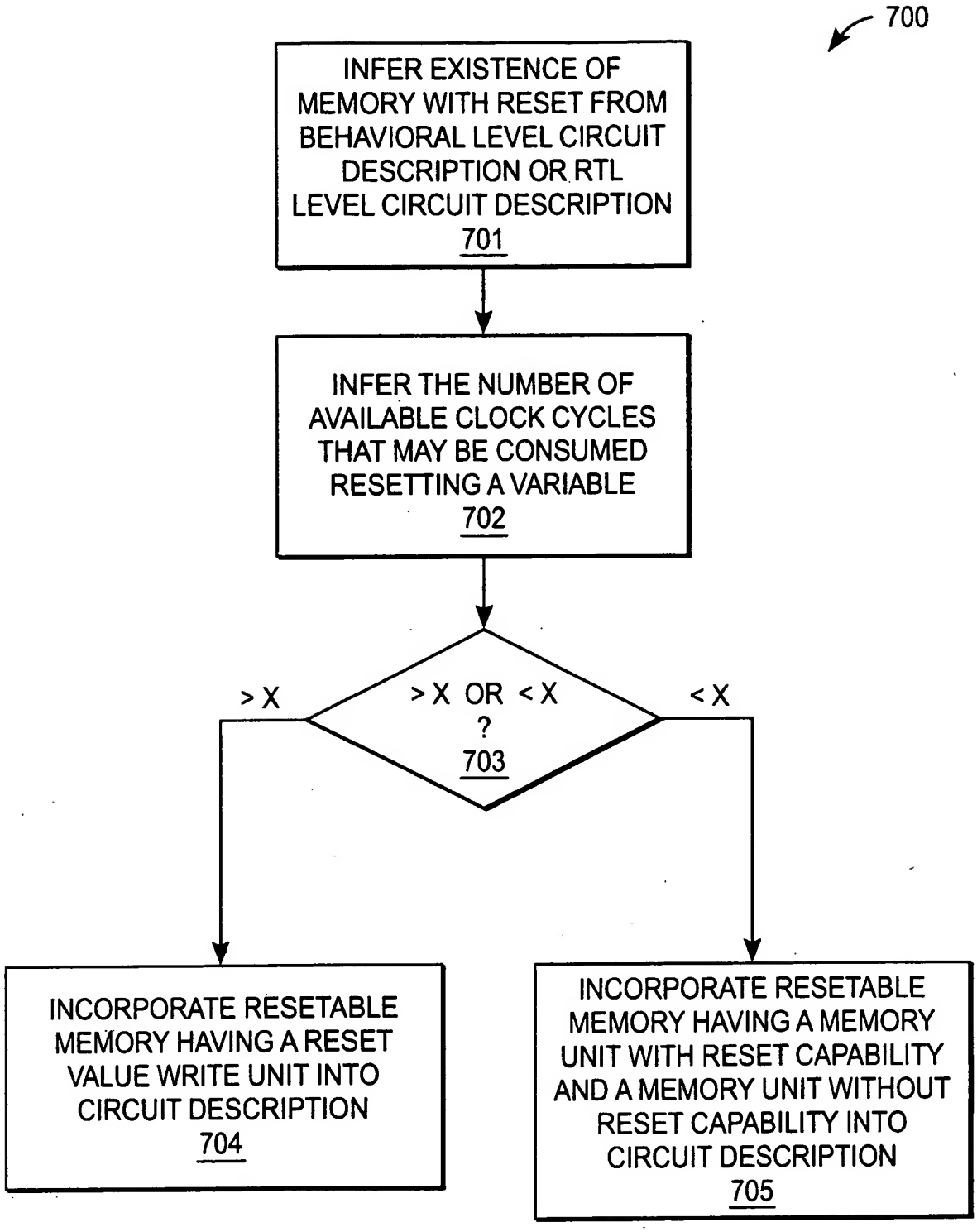
700
INFER EXISTENCE OF MEMORY WITH RESET FROM BEHAVIORAL LEVEL CIRCUIT DESCRIPTION OR RTL LEVEL CIRCUIT DESCRIPTION
701
INFER THE NUMBER OF AVAILABLE CLOCK CYCLES THAT MAY BE CONSUMED RESETTING A VARIABLE
702
> X OR < X ?
703
> X
< X
INCORPORATE RESETABLE MEMORY HAVING A RESET VALUE WRITE UNIT INTO CIRCUIT DESCRIPTION
704
INCORPORATE RESETABLE MEMORY HAVING A MEMORY UNIT WITH RESET CAPABILITY AND A MEMORY UNIT WITHOUT RESET CAPABILITY INTO CIRCUIT DESCRIPTION
705

FIG. 7

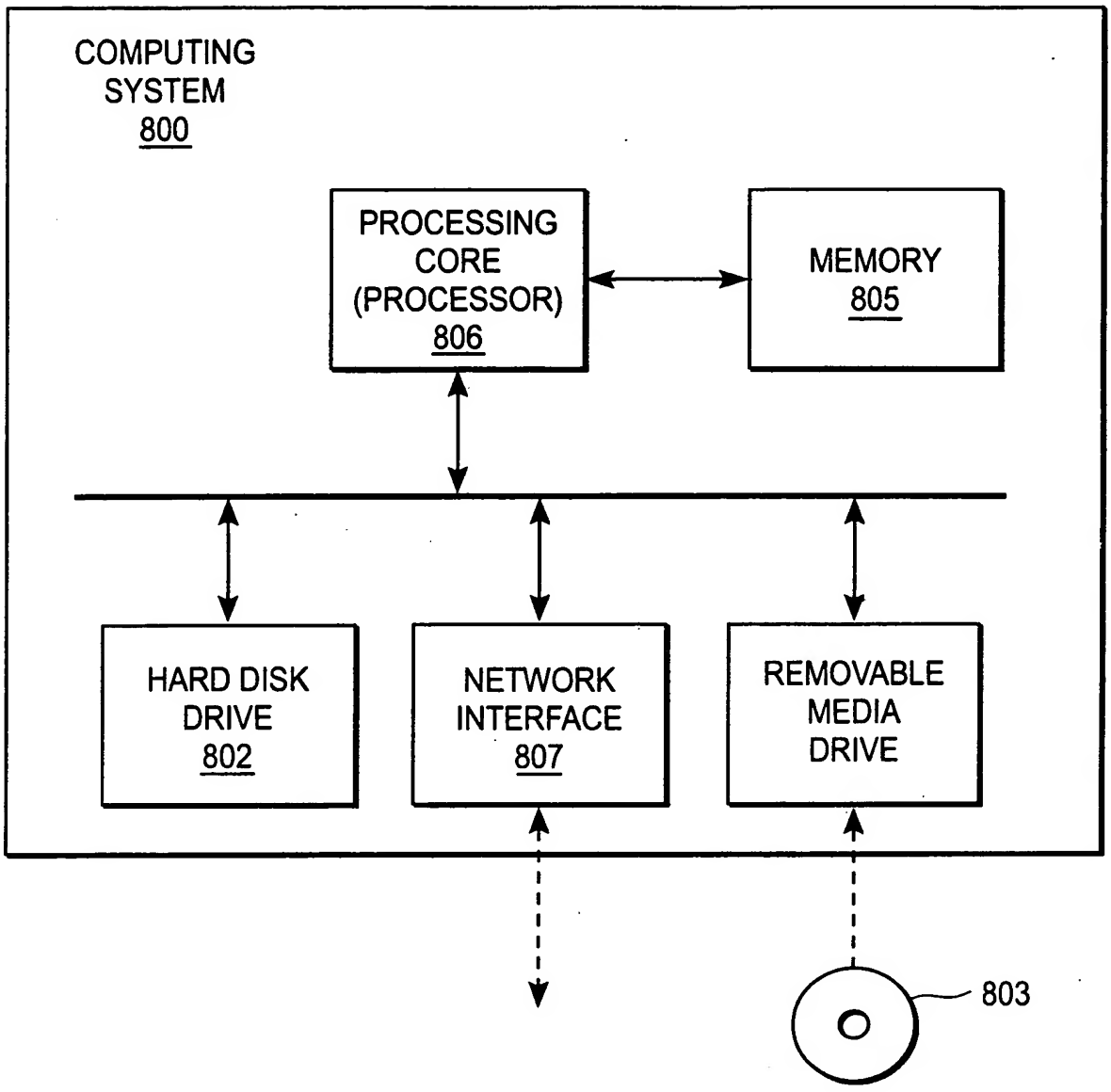
COMPUTING SYSTEM
800
PROCESSING CORE (PROCESSOR)
806
MEMORY
805
HARD DISK DRIVE
802
NETWORK INTERFACE
807
REMOVABLE MEDIA DRIVE
803

FIG. 8